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A Capacitor-Free, Fast Transient Response Linear Voltage Regulator In a 180nm CMOS

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***Abstract*—A 1.8 V capacitor-free linear regulator with fast transient response based on a new topology with a fast and slow regulation loop is presented. The design has been laid out and simulated in a 0.18 μm CMOS process. The design has a low component count and is tailored for system-on-chip integration. A current step load from 0-50 mA with a rise time of 1 μs results in an undershoot in the output voltage of 140 mV for a period of 39 ns. The regulator sources up to 50 mA current load.**

I. Introduction

In contemporary low power CMOS integrated circuits, multiple supply voltages are often a necessity for optimizing chip area and power efficiency. Linear regulators excel at providing low output noise and less electromagnetic emission compared to switching mode regulators. Opposed to switching regulators, linear regulators do not require external inductors and are generally less space consuming. Despite a lower power efficiency, linear regulators can be designed to draw a noticeably low quiescent current, i.e. the sum of bias currents during unloaded conditions, since these designs do not depend on a minimum duty cycle. This is advantageous for handheld systems where most energy is consumed in stand-by mode [1].

Due to a finite bandwidth of linear regulators, conventional designs require a high value buffer capacitor, frequently situated off-chip [2]. In portable devices with strict requirements on space consumption, such as hearing aids or cell phones, usage of discrete components must be minimized. This has lead to the development of numerous capacitor-free regulator topologies [3]–[5]. The external capacitor ensures stability and acts as a supply for the frequency components of the current load, I_L, outside the bandwidth of the regulator. With fast changing current loads an exclusion of the capacitor will lead to large voltage drops on the output and a longer duration of transient recovery, i.e. rise time, T_R.

One approach of avoiding this large capacitor is by emulating the capacitance using an internal operational amplifier-based active circuit as done in [4]. However, the design is rather complex and utilizes a low dropout methodology with a PMOS pass transistor. Considering the lower charge carrier mobility in most PMOS devices, more area is consumed compared to an NMOS with the same drain current. This increases the gate capacitance and leads to a longer T_R. Another approach is to increase the bandwidth of the control loop to a level where the regulator is able to compensate for the fast changing current loads [3]. This is achieved by controlling the pass transistor with a simple single stage error amplifier. In [3] the transient performance is enhanced by an assisting amplifier and the DC output level is stabilized by a low bandwidth amplifier in a parallel control loop.

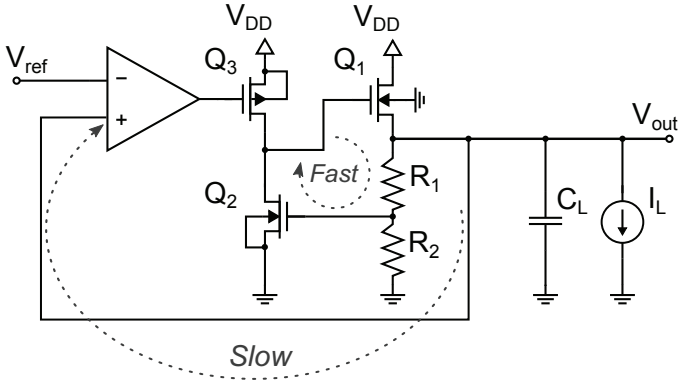


Fig. 1: Functional diagram of the proposed linear voltage regulator

The new design proposed in this work is based on a principle similar to [3], employing two control loops and an NMOS pass transistor configured as a source follower (SF). Refer to Fig. 1 for the circuit diagram of the proposed regulator. The design specifications target the following parameters. The regulator is supplied by voltage of 3.3 V and an outputs a voltage of 1.8 V. The regulator can source an I_L of 0-50 mA which can be stepped with a 1 μs rise -and fall time. The output voltage undershoots less than 200 mV during current step load and the circuit consumes less than 100 μA without load. A C_L of 1 pF or less will not cause ripple on the output. The design is intended for small products like hearing aids. All transistors in the circuit are 5 V MOSFETs.

II. Circuit Description

The fast loop consists of a common source (CS) amplifier, Q_2 and Q_3, driving the pass transistor Q_1. The current source Q_3 is controlled by the slow loop comprising the operational amplifier. The proposed design does not contain any large passive devices and has a low count of transistors. Consequently the simplicity allows for easy and space efficient implementation, yet demonstrating good performance. C_L depicts the load capacitance The following sections describe the two control loops in detail. A full circuit diagram is depicted on Fig. 2.

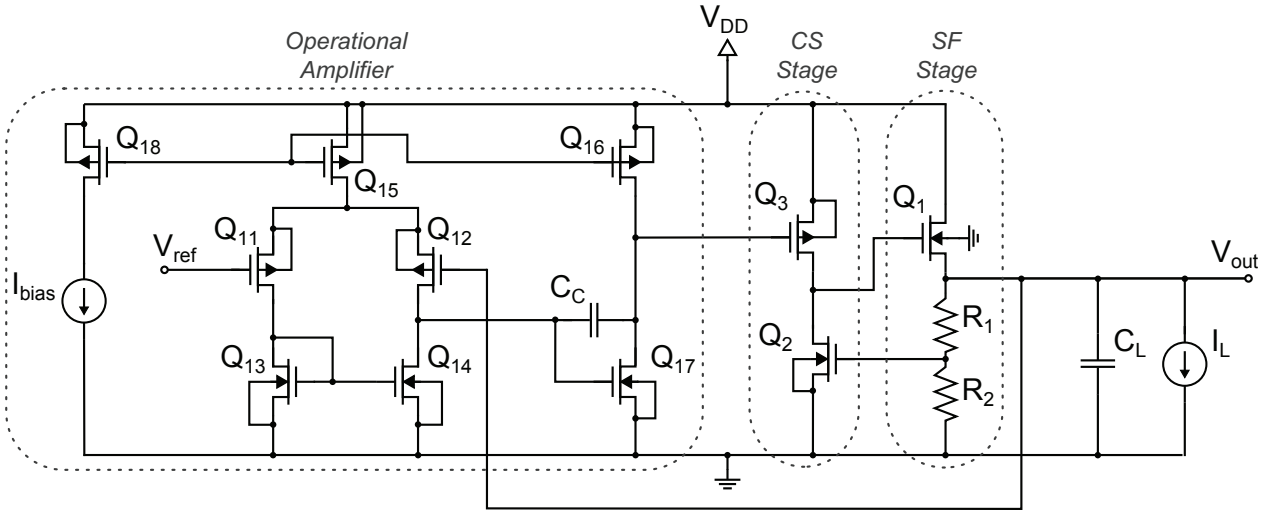


Fig. 2: Full schematic of the proposed linear regulator

A. Fast Loop

By assuming the fast loop constitutes an underdamped system, the gain bandwidth product (GBWP) of the open loop gain will be inversely proportional to T_R. The open loop starts at the gate of Q_2 and ends at the source of Q_1 Based on the former assumption, an uncompensated error amplifier with a maximized $GBWP/I_D$ can be employed in order to exploit most of the quiescent current for control speed. I_D is the drain current, here spent in the gain stage of the amplifier.

$$A_{OL}(s) = \left(\frac{g_{m2}R_{cs}R'_L}{R'_L + 1/g_{m1}}\right)\frac{\left(1+\frac{s}{\omega_z}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)} \quad (1)$$

$$\textit{where } R'_L = (R_1+R_2)||r_{ds1}||(1/g_{s1})$$

$$\omega_{p1} = \frac{(1/R_{cs})(g_{m1}+1/R'_L)}{C'_L/R_{cs} + C_1(g_{m1}+1/R_{cs}) + C_{gs1}/R'_L} \quad (2)$$

$$\omega_{p2} = \frac{C'_L/R_{cs} + C_1(g_{m1}+1/R_{cs}) + C_{gs1}/R'_L}{C_{gs1}C'_L + C_1(C_{gs1}+C'_L)} \quad (3)$$

$$\omega_z = g_{m1}/C_{gs1} \quad (4)$$

The open loop transfer function, $A_{OL}(s)$, is described in (1) where R_{cs} is the output resistance of the CS stage, C'_L is C_L plus the source-bulk capacitance of Q_1, C_{gs1} is the gate-source capacitance and C_1 is the gate-bulk and gate-drain capacitance of Q_1. r_{ds1} is the output resistance and g_{s1} is the body transconductance of Q_1.

Since the CS stage delivers the gain of fast loop the transconductance of Q_2, g_{m2}, must be maximized to achieve the greatest GBWP. Correspondingly R_1 and R_2 are used to decrease the gate voltage of Q_2 and thereby drive it into moderate inversion for a higher g_m. These resistors also bias Q_1. The optimum current distribution in the CS and SF, that resulted in the shortest T_R, was found empirically. The gate-source voltage of Q_1, V_{gs1}, becomes considerably large at maximum I_L. The body effect additionally increases V_{gs1}, so Q_1 must have a very high W/L to keep Q_3 in saturation. This vast device area introduces substantial parasitic capacitances in Q_1 which will dominate the frequency response of the fast loop in terms of C_1 and C_{gs1}. To minimize T_R, the dimensions of Q_1 must therefore be kept as low as the effective voltage, V_{eff}, of Q_3 allows it. At maximum I_L the drain-source voltage of Q_3 will be at its minimum and will be the limiting factor when choosing the supply voltage. However, if a slightly lower voltage domain is available, it can be connected to the drain of Q_1. In that way the power dissipated in Q_1 can be significantly reduced without sacrificing performance. Another limiting factor is the load capacitance. As seen in (2) and (3), greater values of C_L will push the poles down in frequency and potentially closer together, and therefore at some point compromise the system stability. This significantly determines the maximum amount of devices that the linear regulator can supply.

The loop gain of the fast loop is defined as $L(s) = A_{OL}(s)\frac{R_2}{R_1}$. When current step loads are applied, ringing can occur on the output of the regulator due to insufficient phase margin of the loop response. Therefore it is desirable to keep the phase margin of $L(s)$ above 75 degrees at maximum expected load capacitance.

B. Slow Loop

The role of the slow loop is to control the gate voltage of Q_3 and thereby stabilize the DC level at V_{out}. The well known Miller compensated, two stage operational amplifier (opamp) has been utilized for this function. Transistor Q_{11} to Q_{18} and C_C constitute the opamp. The slow loop starts at the gate of Q_{12}, then goes through the opamp, from gate to the source of Q_3 and then from the gate to the source of Q_1.

In order not to degrade the frequency response of the fast loop, this opamp has a unity gain frequency approximately two decades below the one of the fast loop; wherefore the opamp does only require a minimal bias current. When greater

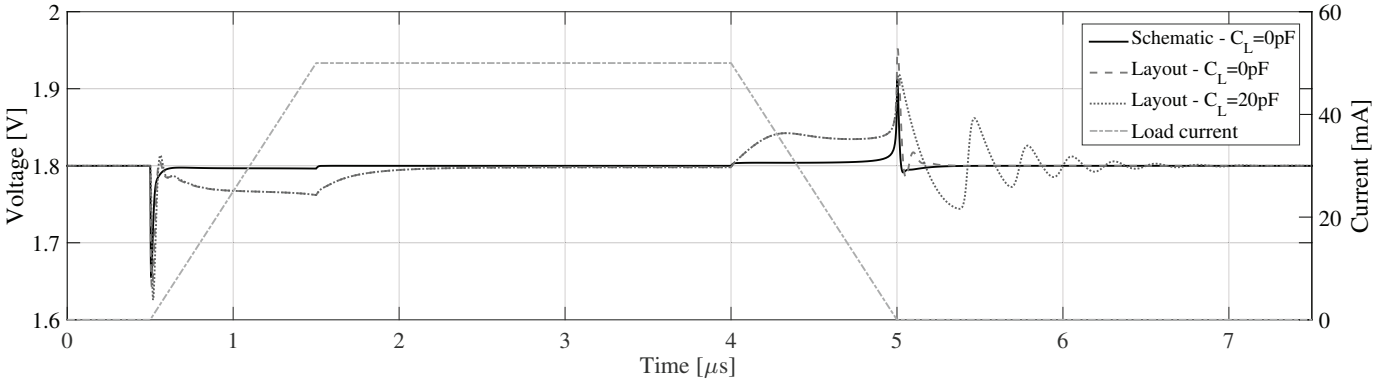
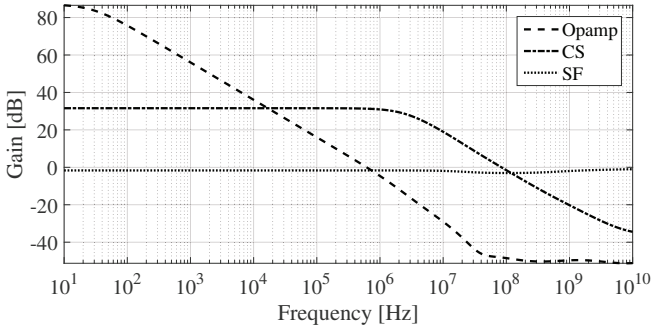
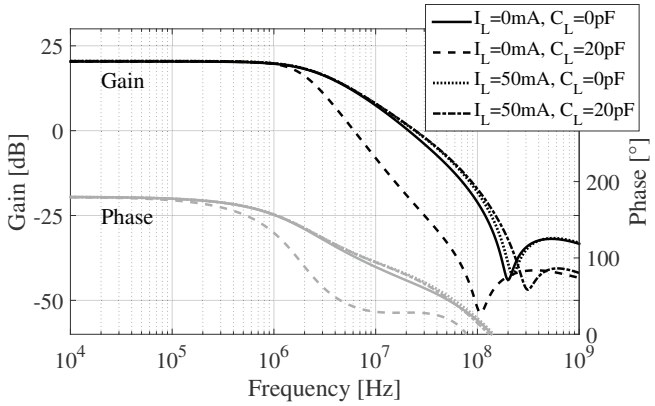


Fig. 4: Transient response with closed slow and fast loop, simulation with and without extracted parasitics



(a) Frequency response of the operational amplifier, the common source stage (Q_3 isolated from the opamp) and the source follower stage, all without extracted parasitics. $C_L = 0$ and $I_L = 0$



(b) Transfer function of L(s) (Q_3 isolated from the opamp), with and without capacitive and current load, all without extracted parasitics

Fig. 3: Simulation results of the proposed linear regulator

steps in I_L occur the opamp must be able to drive the gate of Q_3 without slewing the transient. Therefore, the common source stage of the opamp must provide a sufficiently large drain current of Q_{16}, I_{D16}. The required I_{D16} can be reduced by choosing a lower W/L for Q_3 to reduce the parasitic capacitance related to the gate. A shorter channel length of Q_3 will reduce R_{cs} and thereby decrease ω_{p1} which will lead to a lower GBWP. Chosing W_3/L_3 is consequently a compromise between GBWP of the CS stage, V_{gs} of Q_3, which also dictates W_1/L_1, and finally the necessary I_{D16} to reduce slewing.

The design compromises of the slow and fast loop discussed above lead to the device dimensions and drain currents presented in Table I. A value of 300 fF was chosen for C_C.

III. Simulation Results

The proposed capacitor-free linear voltage regulator has been implemented on schematic and layout level in a 0.18 μm CMOS process. The presented results are from the typical temperature and process corner. The most advantageous bias current distribution has been fine tuned by simulation to yield the fastest T_R. As a result, 82.2 μA is distributed to the CS stage, 10 μA to the SF stage and 5.8 μA to the opamp, giving a total quiescent current consumption of 98.4 μA.

The layout is presented in Fig. 4 and has been designed for optimized chip area and measures 150 μm x 42 μm. Common centroid matching and dummy devices have been used where necessary and possible. Due to the extremely low W/L of the devices in the opamp, it has not been possible to use unit transistors in the design. The enormous transistor in the left part is Q_1 with dimensions $3000\mu m/0.7\mu m$.

TABLE I: Device dimensions and drain current

Device	Width [μm]	Length [μm]	$I_{quiescent}$ [μA]
Q_1	3000	0.7	10
Q_2	84	0.7	82.2
Q_3	140	0.6	82.2
$Q_{11,12}$	1	1	0.075
$Q_{13,14}$	0.5	4	0.075
Q_{15}	0.5	1	0.15
Q_{16}	30	1	5.5
Q_{17}	5	1	5.5
Q_{18}	0.5	1	0.15

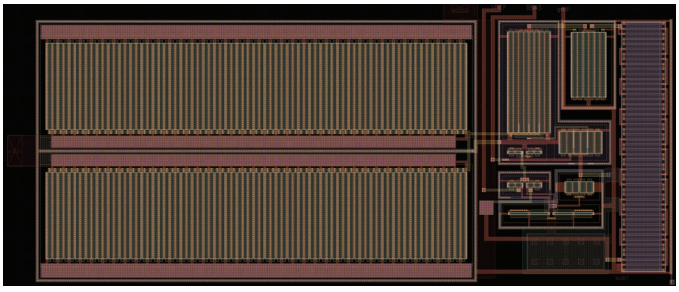


Fig. 4: Screenshot of the layout of the proposed linear regulator

Post-layout simulation has been performed to account for parasitic components in the layout. The frequency responses of the individual circuit segments and the closed loop gain are depicted on Figs. 3a and 3b. It appears that loading the linear regulator by 20 pF will result in an underdamped response due to a phase margin of around 30 degrees. A transient analysis has been performed on schematic and the post-simulated layout level. The circuit was tested with a current step load of 0-50 mA with a rise -and fall time of 1 μs. The transient performance is showed on Fig. 4. When simulating with the extracted parasitics, the transient response exhibit a larger and longer voltage drop during transitions in the current step load. This drop might be caused by the capacitance between the metal layers and poly covering the large drain-source and gate area of Q_1 respectively. It should be noted that the size of the current step represents a worst case scenario. Under typical circumstances smaller load steps are expected. When a 20 pF load is applied, oscillations occur during step down of I_L. Referring to Fig. 3b, this response is expected due to the low phase margin. The oscillations only occur during load stepdown because g_{m1} decreases with the current in Q_1 and thereby moves ω_{p2} down in frequency according to (3). A higher immunity to C_L is conclusively obtained with a greater g_{m1}. A T_R of 39 ns is obtained from the schematic level simulations. When simulating with the extracted parasitics included T_R increases to 1.158 μs. This is a significant difference that indicates layout improvements could better the performance. The voltage undershoot is 140 mV for the schematic and 160 mV for the layout. If the duration of the load step is reduced to 10 ns, a T_R of 20.4 ns is obtained with a 640 mV undershoot on schematic level. Simulations showed that rise times of the load step greater than 1 μs would result in even lower undershoot voltages.

IV. Discussion

The presented theory and results of the proposed linear voltage regulator show that an bulky external capacitor can be replaced by a fast control loop. Due to the sensitivity to larger load capacitances, the regulator should supply internal circuitry only. The chip area of the proposed design is fairly small when comparing to the other designs in Table II. Also the design is simple to implement, which makes it ideal for a system-on-chip designs. The simulation results from the schematic level and extracted layout simulations of the proposed design are summarized in Table II for comparison with other designs. A figure of merit (FOM) from [1] is used for standardized comparison and appears in (5). As seen, (5) focuses on how fast a system can be made with a certain current efficiency. The smaller the FOM, the better the regulator.

$$FOM = T_R \frac{I_{quiescent}}{I_{L,max}} \tag{5}$$

The chip area consumed by this design is considerably smaller than [3] and comparable with [1]. Assuming the layout was optimized and matched the performance on schematic level, the results of this work show a promising performance in terms of FOM compared to [4] and [3]. This topology can also be designed to drive greater capacitive loads which can be achieved by increasing the current in Q_1 for a higher g_{m1}.

TABLE II: Comparison with other designs

	[1]	[4]	[3]	This work	
				Schematic	Layout
Active area	0.0040 mm^2	-	0.08 mm^2	-	0.0093 mm^2
Supply	1.2 V	-	1.8 V/3.6 V	3.3 V	3.3 V
Output	0.9 V	2.5 V	1.2 V	1.8 V	1.8 V
$I_{quiescent}$	6 mA	80 uA	132 uA	98.4 uA	98.3 uA
Imax	100 mA	100 mA	200 mA	50 mA	50 mA
I_L **Rise time**	100 ps	10 us	1 us	1 us	1 us
T_R	0.54 ns	15 us	200 ns	39 ns	1.16 μs
Undershoot	90 mV	60 mV	16 mV	140 mV	160 mV
FOM	0.032 ns	11.2 ns	0.132 ns	0.077 ns	2.281 ns
Decoupling	0.6 nF	-	-	-	-

V. Conclusion

A new capacitor-free linear voltage regulator utilizing multi-loop control, suited for small system-on-chip applications, was designed. With its fast transient performance it demonstrated results comparable to or better than other similar designs from the literature. Simulation results showed that an undershoot of 140 mV with a rise time of 39 ns occured when a 1 μs load transient variation from 0-50 mA was applied.

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